AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A bus controller ~~that controls~~ for controlling processing levels of plural requesters which access a common memory, the bus controller including:

an access cycle counter for counting the number of access cycles for which the common memory is accessed;

an arbiter coupled to the access cycle counter for judging a processing level of a processing of a requester, ~~means for performing a processing of a processing level that is selected~~ from plural processing levels that are different dependent on each requester, for which an access permission is given, and for performing the processing of the processing level that is judged previously;

a correspondence information unit coupled to the arbiter for storing correspondence information that shows correspondences between the plural processing levels of the respective requesters and the access cycle numbers, [[;]]

~~a processing level judging means for indicating a processing level of the processing performed by the processing means of the respective requesters for which an access permission is given; and~~

wherein the arbiter is operable to judge ~~said processing level judging means indicating~~ the processing levels of the respective requesters for which an access permission is given, in accordance with a present cycle number that is counted by the access cycle counter, the number of remaining cycles up to a predetermined limit cycle number, and the correspondence information showing the correspondences between the processing levels of the respective requesters and the access cycle numbers.

2. (Currently Amended) A bus controller ~~that arbitrates~~ for arbitrating plural access requests which are issued from plural requesters ~~that would~~ to access a common memory, the bus controller including:

an access cycle counter for counting the number of access cycles for which the common memory is accessed;

a correspondence information unit for storing correspondence information that shows correspondences between the plural processing levels of the respective requesters and the access cycle numbers; and

an arbiter coupled to the access cycle counter and the correspondence information unit ~~that arbitrates~~ for arbitrating the plural access requests which are issued from the plural requesters, ~~requesters; and~~

wherein said arbiter ~~performing~~ is operable to perform a control for giving no permission to a non-realtime bus access request when it is expected that a total number of cycles of all the requesters would exceed ~~the~~ a limit cycle number in accordance with a present cycle number that is counted by the access cycle counter, the number of remaining cycles up to a predetermined limit cycle number, and the correspondence information that shows correspondences between the plural requesters and the access cycle numbers.

3. (Currently Amended) A bus controller ~~that controls~~ for controlling processing levels of plural requesters which access a common memory, and ~~arbitrates~~ for arbitrating plural access requests that are issued from the plural requesters, the bus controller including:

an access cycle counter for counting the number of access cycles for which the common

memory is accessed;

~~a processing means for performing a processing of a processing level that is selected from plural processing levels which are different dependent on each requester;~~

an arbiter coupled to the access cycle counter for judging a processing level of a processing requester, from plural processing levels that are different dependent on each requester, for which an access permission is given for performing the processing of the processing level that is judged previously, and for arbitrating the plural access requests which are issued from the plural requesters to access the common memory; and

a correspondence information unit coupled to the arbiter for storing correspondence information that shows correspondences between the plural processing levels of the respective requesters and the access cycle numbers[[;]],

~~a processing level judging means for indicating a processing level of the processing performed by the processing means of the respective requesters for which an access permission is given;~~

~~an arbiter for arbitrating the plural access requests which are issued from the plural requesters which would access the common memory, and~~

wherein the arbiter is operable to judge the processing levels ~~said processing level judging means and said arbiter indicating the levels of the processings which are performed by the processing means~~ of the respective requesters for which an access permission is given, in accordance with a present cycle number counted by the access cycle counter, and the number of remaining cycles up to a predetermined limit cycle number ~~number, and the correspondence information, and performing a control for giving no permission to a non-realtime bus access~~

~~request when it is expected that a total number of cycles of all requesters would exceed the limit cycle number~~.

4. (Currently Amended) The bus controller of Claim 1, ~~including:~~

~~the processing level judging means~~

wherein the arbiter is operable to calculate ~~calculating~~ a total sum of the numbers of access cycles when performing processings from a processing of a requester, which is two processings after a present one, to the last processing in a reference time, at levels for which the respective maximum cycle numbers are the smallest,

wherein the arbiter is operable to obtain ~~obtaining~~ the number of remaining cycles by subtracting a present access cycle number from the limit cycle number, and

wherein the arbiter is operable to select ~~selecting~~ a processing level of a next processing of a requester within a range of the cycle number that is obtained by subtracting the total sum from the number of the remaining cycles.

5. (Currently Amended) The bus controller of Claim 2, ~~including:~~

wherein the arbiter is operable to calculate ~~calculating~~ a total sum of the numbers of access cycles when performing processings from a next ~~processing of a non-realtime requester as a next~~ requester to the last processing in a reference time, at levels for which the respective maximum cycle numbers are the smallest,

wherein the arbiter is operable to obtain ~~obtaining~~ the number of remaining cycles by subtracting a present access cycle number from the limit cycle number, and

wherein the arbiter is operable to perform ~~performing~~ a control for giving no permission to the non-realtime requester when the processings cannot be completed within a range of the cycle number that is obtained by subtracting the total sum from the number of remaining cycles.

6. (Currently Amended) The bus controller of Claim 3, ~~including:~~

~~the processing level judging means and the arbiter~~

wherein the arbiter is operable to calculate a total sum of the numbers of access cycles when performing processings from a next processing of a non-realtime requester as a next requester to the last processing in a reference time, at levels for which the respective maximum cycle numbers are the smallest,

wherein the arbiter is operable to obtain ~~obtaining~~ the number of remaining cycles by subtracting a present access cycle number from the limit cycle number, and

wherein the arbiter is operable to perform ~~performing~~ a control for giving no permission to the non-realtime requester when the processings cannot be completed within a range of the cycle number that is obtained by subtracting the total sum from the number of remaining cycles.

7. (Currently Amended) The bus controller of Claim 6, wherein

the non-realtime requester has plural different processing levels.